LISTING OF CLAIMS

No amendments to the claims are presented in this Response. This listing of claims is provided as a convenience to the Examiner and will replace all prior versions, and listings, of claims in the application:

1. (Original) A method for managing data in a register, comprising:

introducing a name level instruction for at least one of a named architected register in a processor;

allowing a programmer to change the current name level of a register name via said name level instruction;

creating a new register with an internal name and a new name level, and

providing a plurality of additional available computer registers.

2. (Original) A method as in claim 1, wherein the name level instruction is used for hardware register renaming.

3. (Original) A method as in claim 2, wherein the name level instruction used for hardware register renaming maintains a pointer to a current physical register for a corresponding architected register.

4. (Original) A method as in claim 1, wherein the name level instruction uses at

least one register stack.

5. (Original) A method as in claim 1, wherein the name level instruction uses a hardware-managed register cache.

6. (Original) A method as in claim 1, wherein the name level instruction uses a hardware-managed special-purpose memory.

7. (Original) A method as in claim 1, wherein the name level instruction uses a hardware-managed component of main storage of a system.

8. (Original) A method as in claim 1, wherein the name level instruction uses a software-managed component of main storage of a system, where upon finding that a name resides in a special purpose area of main storage, an interrupt to the processor causes invocation of an interrupt handler that performs a task of bringing a value of the name level from the main storage to a physical register.

9. (Original) A method as in claim 1, wherein the name level instruction uses a hardware-managed hierarchy of structures such as cache and storage, successively larger in size and slower in access time.

10. (Original) A method as in claim 1, wherein the name level instruction provides for the facilitation of architectural features which overload the architected register namespace reducing the overhead of register management.

11. (Original) A method as in claim 1, wherein the name level instruction provides for additional computer registers without changing the instruction format of the computer.

12. (Original) A computer program product comprising:

a computer usable medium having computer readable program code embodied therein for managing data in a register, the computer readable program code in said computer program product comprising:

computer readable program code for causing a computer to utilize a name level instruction;

computer readable program code for causing the computer to change the current name level of a register name via said name level instruction; and

computer readable program code for causing the computer to create a new register with an internal name and a new name level.

13. (Original) A computer program product as in claim 12, wherein the name

level instruction is used for hardware register renaming.

14. (Original) A computer program product as in claim 12, wherein the name level instruction provides for the facilitation of architectural features which overload the architected register namespace reducing the overhead of register management.

15. (Original) A computer program product as in claim 12, wherein the name level instruction provides for additional computer registers without changing the instruction format of the computer.

16. (Original) A data processor comprising:

a memory;

at least one execution unit operating in cooperation with instructions and comprising circuitry to manage data in a register;

said data processor further comprising a plurality of registers, and

a register renaming mechanism coupled to a stack of register names and responsive to a name level instruction for creating a new register with an internal name and a new name level by changing a current name level of a register.

17. (Original) A data processor as in claim 16, wherein at least one of the registers is a physical register.

18. (Original) A data processor as in claim 16, wherein at least one of the registers is an architected register.

19. (Original) A data processor as in claim 16, wherein said new register is an architected register.

20. (Original) A data processor as in claim 16, wherein the memory includes a backing store.

21. (Original) A data processor as in claim 16, wherein the name level instruction used for hardware register renaming maintains a pointer to a current physical register for a corresponding architected register.

22. (Original) A data processor as in claim 16, wherein the name level instruction provides for creating additional computer registers without changing the instruction format of the computer.